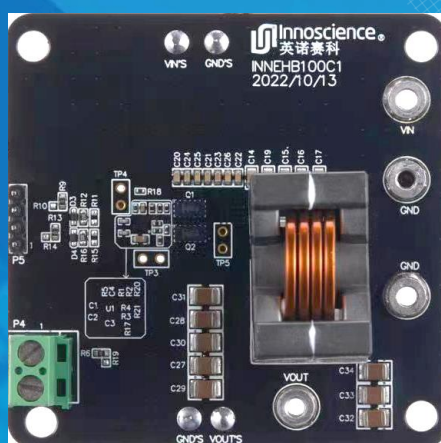# INNEHB100C1

Evaluation Board Manual

100V GaN HEMT INN100W027A

Open Loop Half-Bridge EVB

CAUTION

Please carefully read the following content since it contains critical information about safety and the possible hazard it may cause by

⚠ ELECTRICAL SHOCK HAZARD

There is a dangerous voltage on the demo board, and exposure to high voltage may lead to safety problems such as injury or death.

Proper operating and safety procedures must be adhered to and used only for laboratory evaluation demonstrations and not directly to end-user equipment.

⚠ HOT SURFACE

The surface of PCB can be hot and could cause burns. DO NOT TOUCH THE PCB WHILE OPERATING!!

⚠ REMINDER

This product contains parts that are susceptible to electrostatic discharge (ESD). When using this product, be sure to follow antistatic procedures.

List of Content

1. Overview

1.1. Introduction

INNEHB100C1 is a half-bridge evaluation board equipped with the half-bridge gate driver to evaluate the performance of 100V GaN HEMT INN100W027A. This board can simplify the test process, it can easily realize Buck converter with single or dual PWM input. The evaluation board can be used in BUCK circuit frequency range of 400kHz to 800kHz, input voltage range of 36V to 80V, under the frequency of 600kHz and the wind speed of 1400LFM, 48V-12V full load 23A efficiency can reach 96.70%. The board can be used not only for BUCK circuits, but also for BOOST circuits. The board includes all the necessary information you need, and the layout has been optimized to achieve the best performance. Test points are also included for the waveform measurement and efficiency evaluation.

1.2. Test Equipment Requirement

To evaluate the performance properly, you need to prepare the following test equipment:

1) High speed digital oscilloscope (≥500MHz Bandwidth)
2) Two low voltage DC power supply
3) PWM generator
4) Digital Multimeter
5) DC load (E-load or Power Resistor)

2. Performance summary

Table 1 Electrical Characteristic（Ta=25℃）

Symbol	Parameters	Min	Nom	Max	Units
VDD	VDD supply Voltage	7	8	12	V
Vin	Input Voltage	36	48	80[1]	V
Fsw	Switching frequency		600		kHz
Pout	Output Power			330[2]	W
EFF	Typical efficiency		96.70%[3]		
Vpwm	Input Logic 'High'	3.5		5	V
	Input Logic 'Low'	0		1.5	V

(1) Maximum input voltage depends on inductive loading, maximum switch node ringing must be kept under 100 V for INN100W027A.

(2) Maximum output power with be subject to switching frequency, bus voltage, load current, EVB temperature and thermal cooling.

(3) 96.70% is the efficiency at 48V to 12V, load 23A, frequency 600 kHz, and the wind speed of 1400LFM.
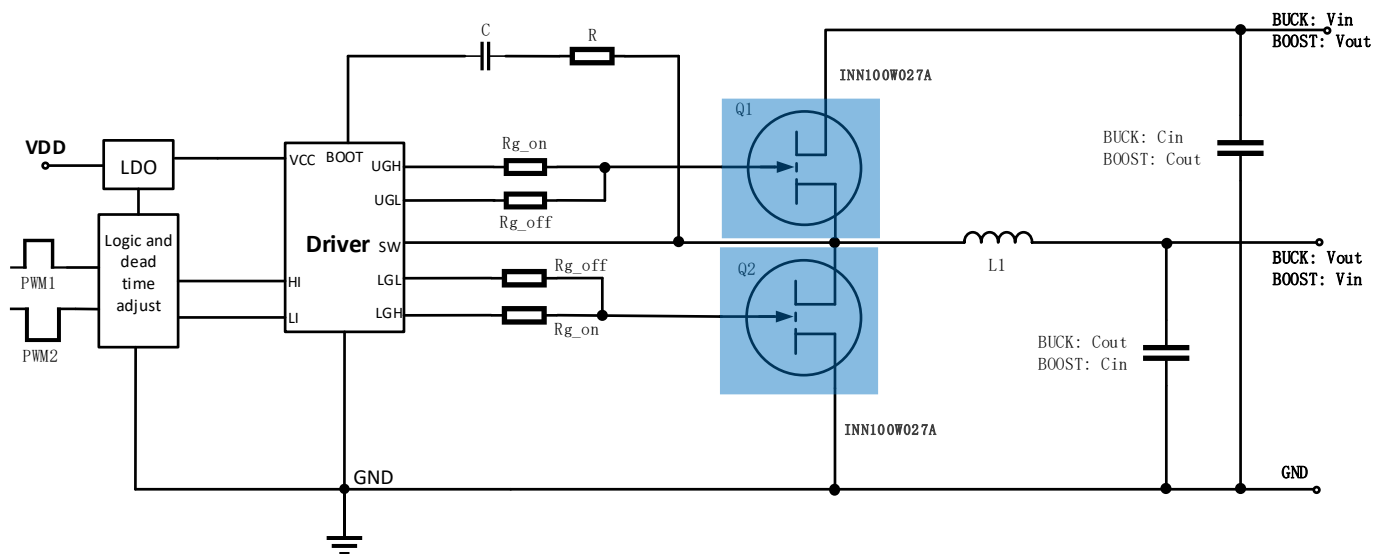
3. Block Diagram

Figure 1 INNEHB100C1 Block Diagram

4. EVB Overview and Schematic
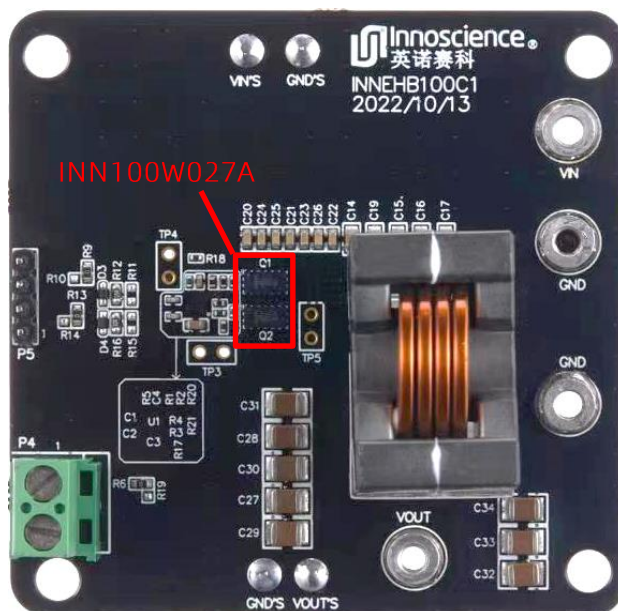
4.1. EVB Overview

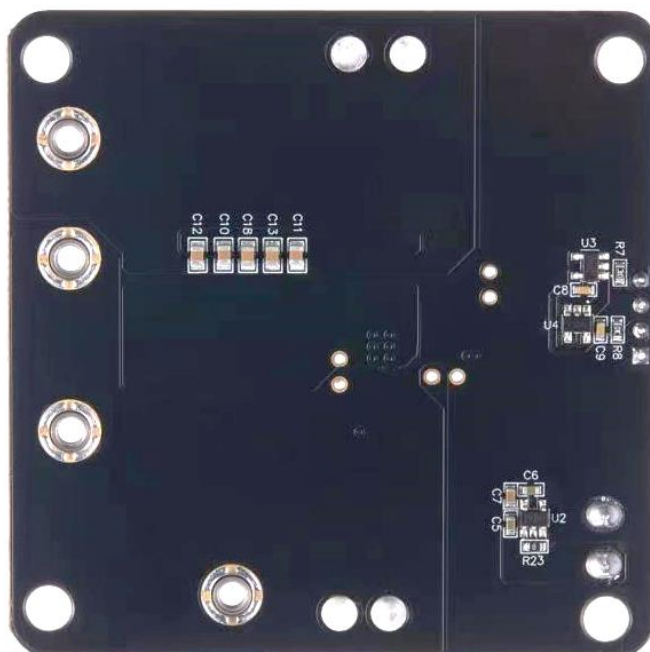Figure 2 Top view of INNEHB100C1

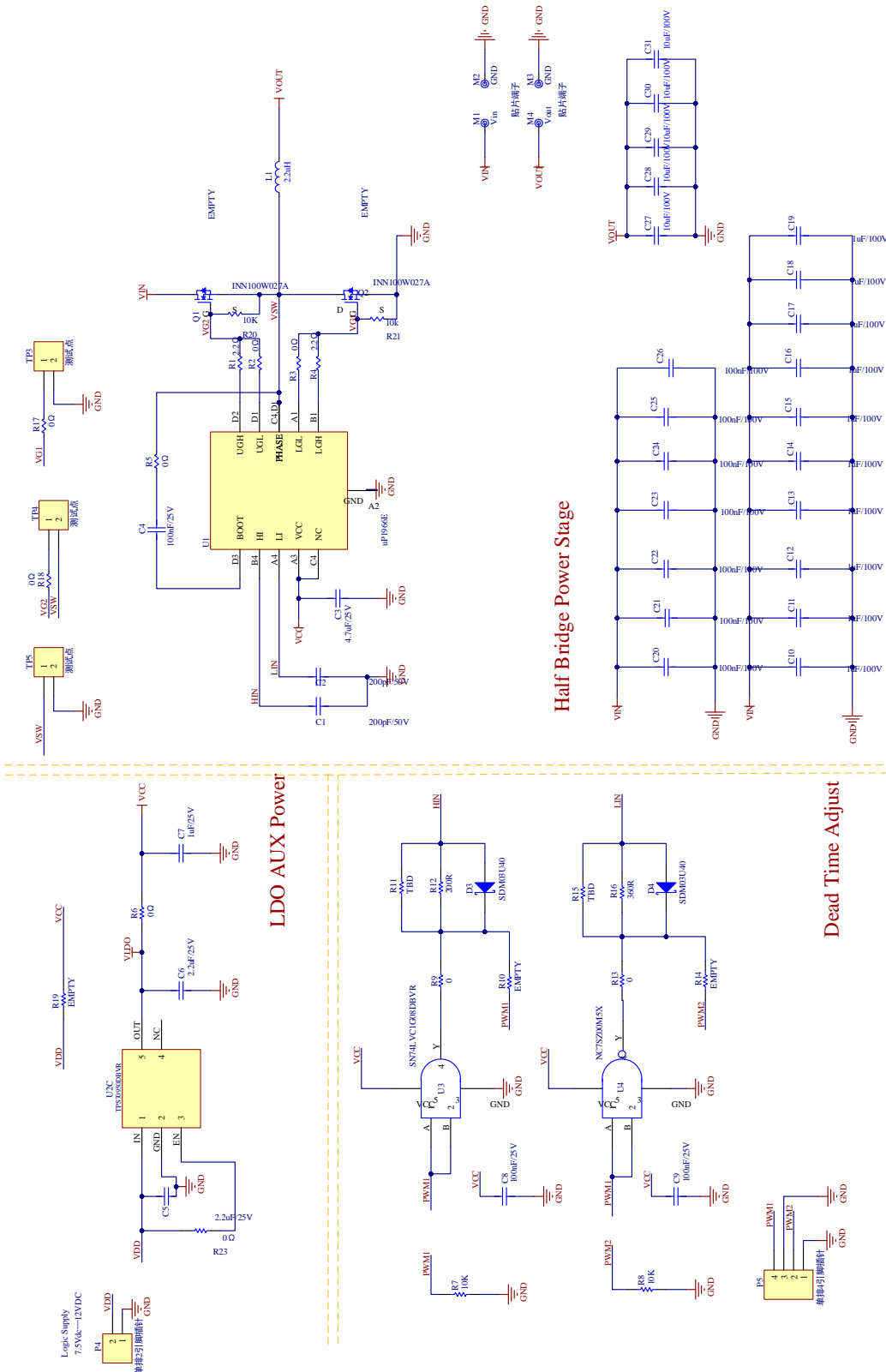Figure 3 Bottom view of INNEHB100C1

4.2. Schematic

Figure 4 Schematic

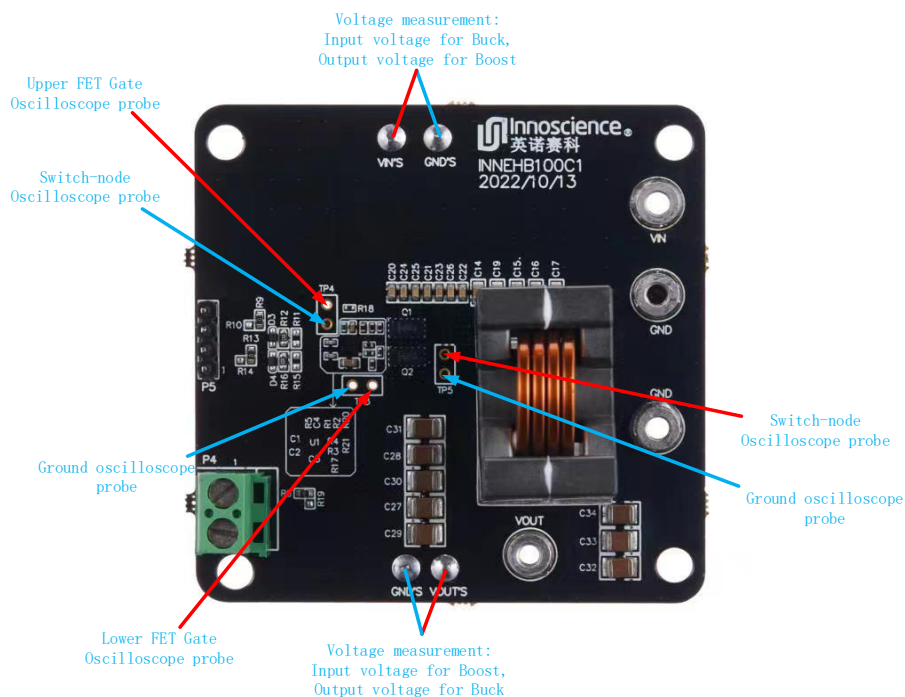## 5. Testing Guide

5.1. Test point location

Figure 5   Measurement points

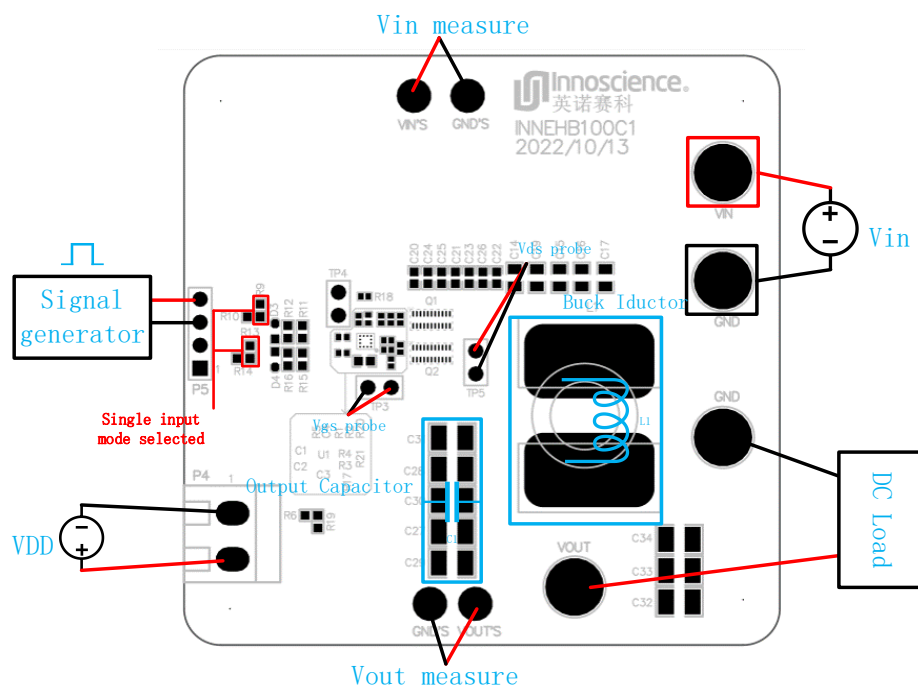### 5.2. Test setup

5.2.1.   Buck Mode
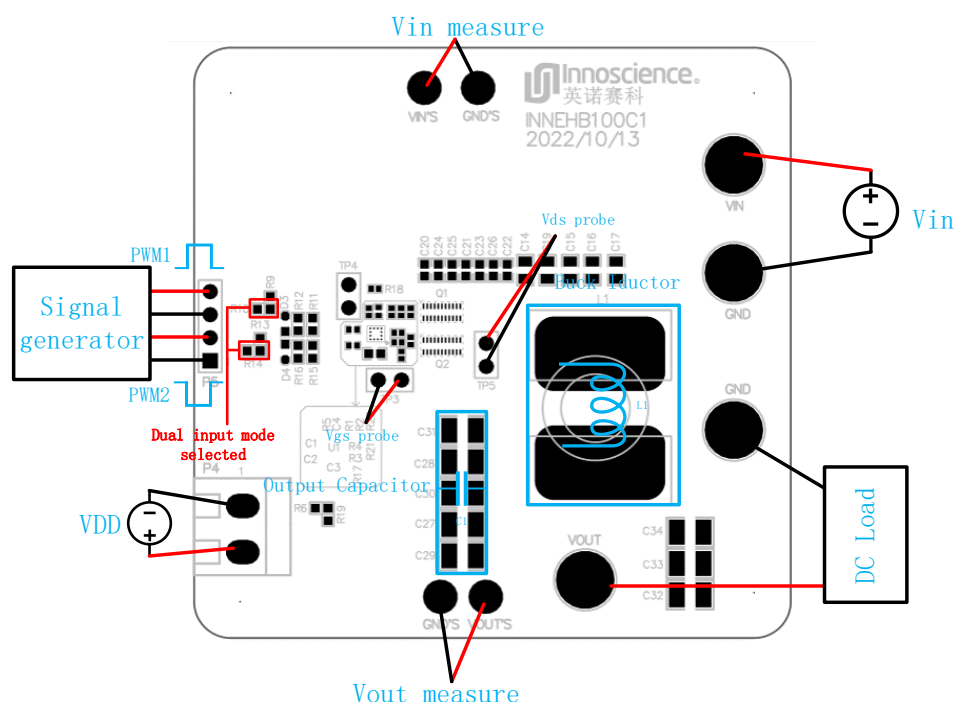
Figure 6 Single-PWM input Buck mode

Figure 7 Dual-PWM input Buck mode

Before tests, single or dual PWM input modes could be selected. When selecting the single PWM input mode, please solder 0Ω resistor to R9 & R13. The dead time is regulated by R12, R16, C1 and C2. The value for R12 is 200Ω, and R16 is 360Ω. The value of C1 and C2 is 200 pF. At this time, at the load of 10A, the corresponding measured dead time between lower FET shutdown and upper FET opening is about 10ns, and the dead time between upper FET shutdown and lower FET opening is also about 10ns.

To select dual PWM mode, please solder 0Ω resistor to R10, R14, R12 and R16. Figure 7 Dual-PWM input Buck mode shows the required PWM signals; PWM1 and PWM2 should be complementary. The dead time is controlled by the signal generator.
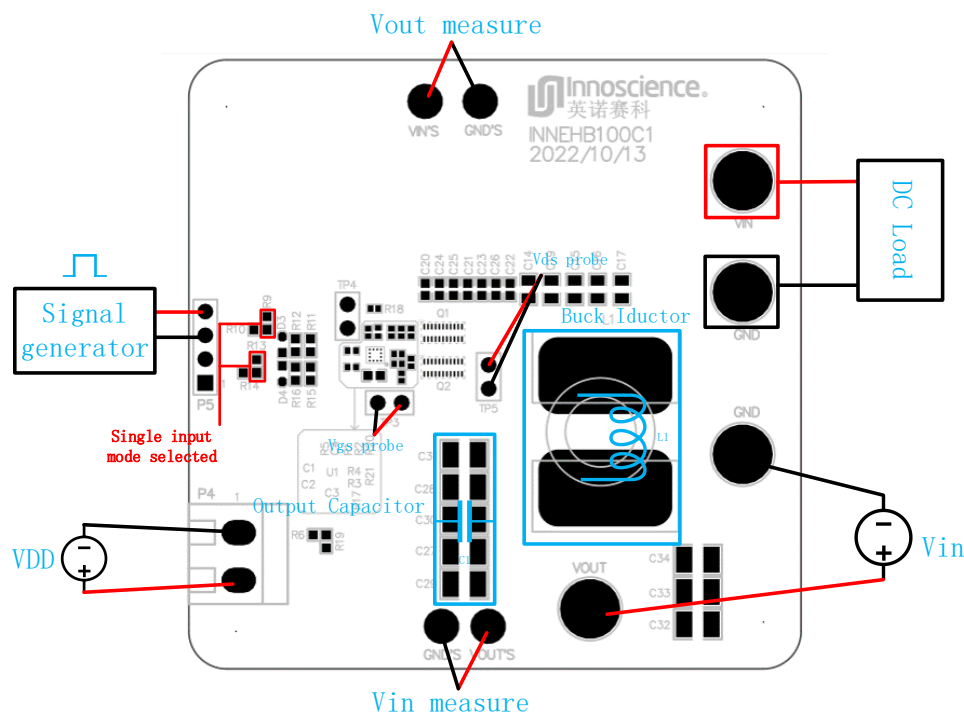
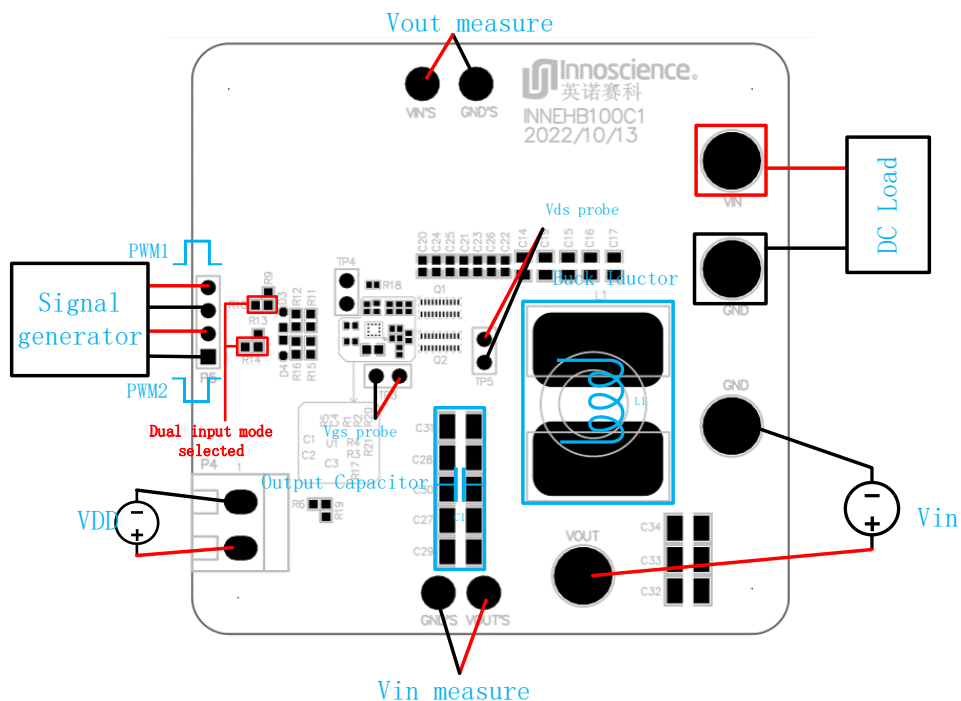## 5.2.2. Boost Mode

Figure 8 Single-PWM input Boost mode

Figure9 Dual-PWM input Boost mode

5.3. Power up and down sequence

5.3.1. Power-up sequence (Buck Mode)

1. Check every power supply is **off.**

2. Connect the DC voltage source to terminal **VIN** and common ground terminal **GND**, as shown in Figure 6 (Pay attention to the polarity).

3. Connect the electronic load to pin **VOUT.**

4. Connect the auxiliary source to the VDD terminal **P4** (Pay attention to the polarity).

5. Connect the signal generator to pin **P5**.

6. Turn on the auxiliary power supply. Note the voltage ranges from 7V ~ 12V.

7. Open the signal generator and enter the PWM signal with the required duty ratio and frequency.

8. Make sure the initial input supply voltage is 0 V, turn on the power and slowly increase the voltage to the desired value (do not exceed the absolute maximum voltage). Probe switch-node and view the switching operation.

9. Once operational, according to the heating state of the device slowly increase the load current, do not exceed the maximum temperature required by the device specification.

5.3.2. Power-up sequence (Boost Mode)

1. Check every power supply is **off**

2. Connect the DC voltage source to pin **VOUT**, as shown in Figure 8 (Pay attention to the polarity).

3. Connect the positive pole of the electronic load to pin **VIN** and the negative pole to pin **GND**.

4. Connect the auxiliary source to the VDD terminal **P4** (Pay attention to the polarity).

5. Connect the signal generator to pin **P5**.

6. Turn on the auxiliary power supply. Note the voltage ranges from 7V ~ 12V.

7. Open the signal generator and enter the PWM signal with the required duty ratio and frequency.

8. Make sure the initial input supply voltage is 0 V, turn on the power and slowly increase the voltage to the desired value (do not exceed the absolute maximum voltage). Probe switch-node and view the switching operation.

9. Once operational, according to the heating state of the device slowly increase the load current, do not exceed the maximum temperature required by the device specification.
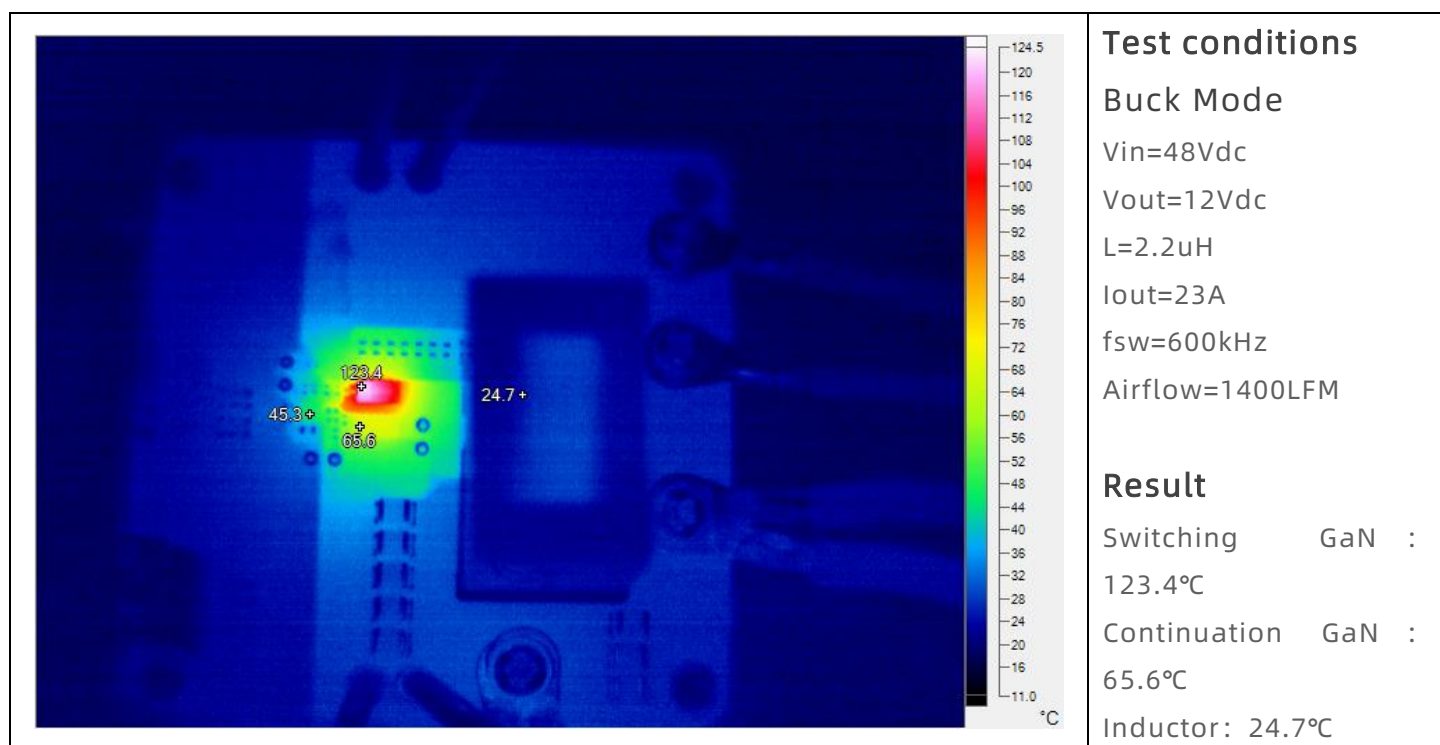
5.3.3. Power-down sequence

1. Turn off the **E-load** first

2. Turn off the **DC voltage source**

3. Turn off the **PWM generator**

4. Turn off the **auxiliary power supply**

6. Evaluation Results

6.1.1. Efficiency Results

Test conditions

Buck Mode

Vin=48Vdc

Vout=12Vdc

L=2.2uH

fsw=600kHz
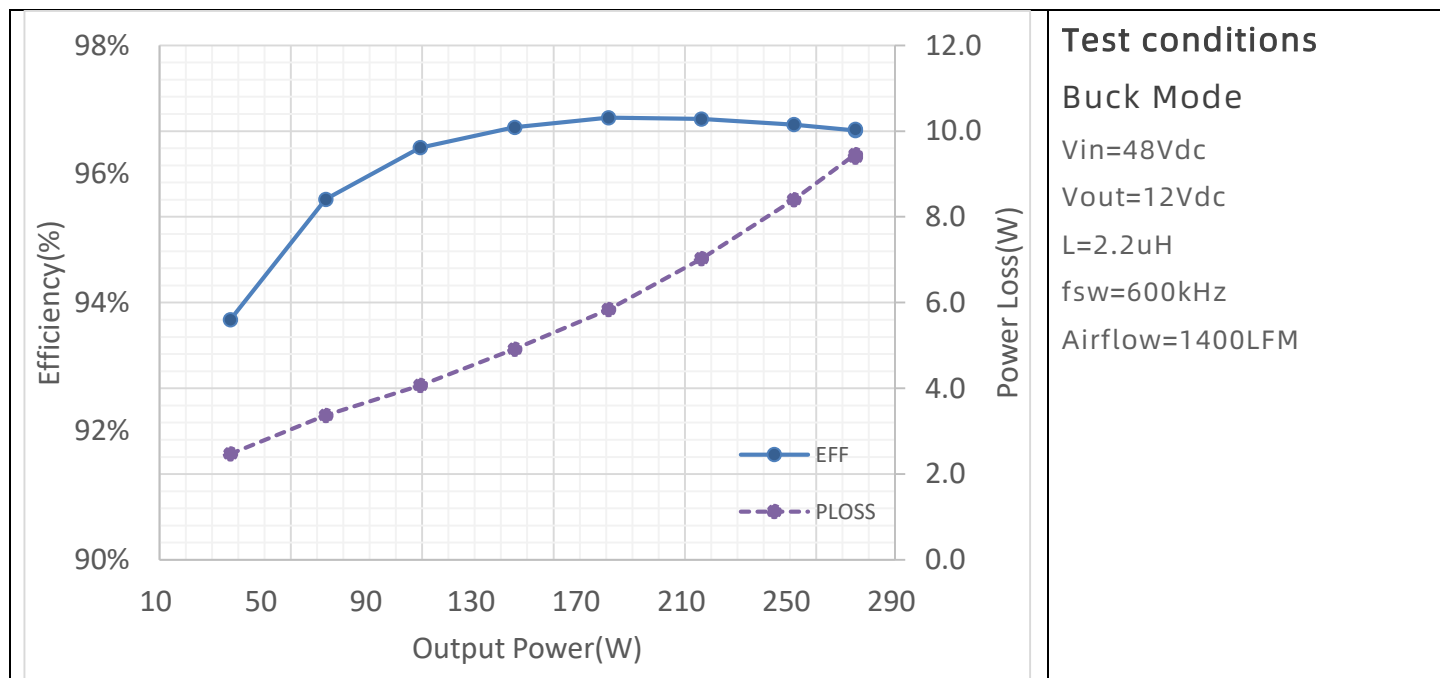
Airflow=1400LFM

6.1.2. Thermal performance

Test conditions

Buck Mode

Vin=48Vdc

Vout=12Vdc

L=2.2uH

Iout=23A

fsw=600kHz

Airflow=1400LFM

Result

Switching GaN : 123.4℃

Continuation GaN : 65.6℃

Inductor: 24.7℃

6.1.3. Switching Waveforms
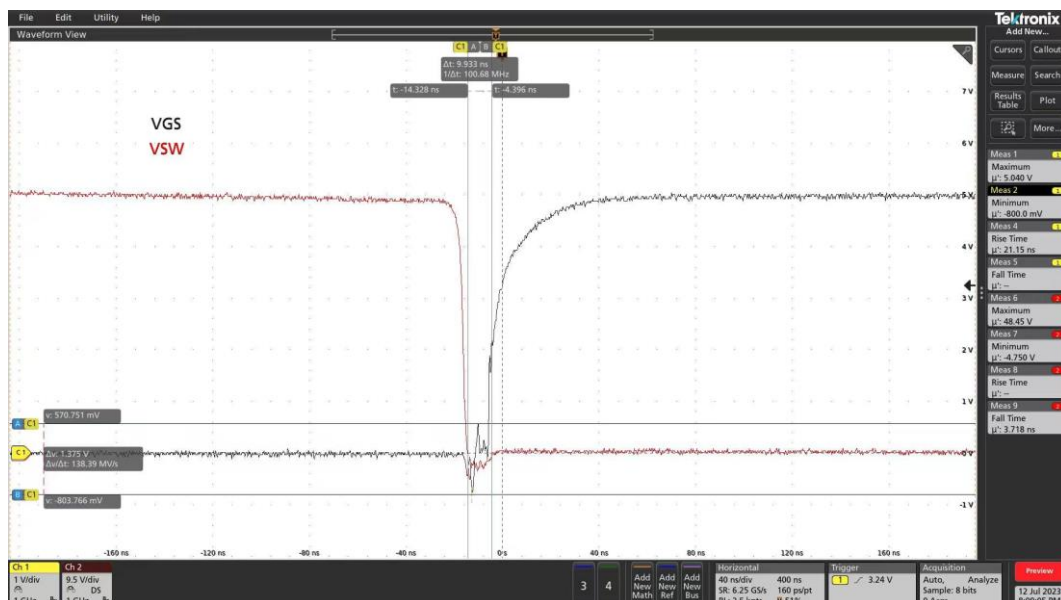
Test conditions

Buck Mode

Vin=48Vdc

Vout=12Vdc

Iout=23A

fsw=600kHz

Airflow=1400LFM

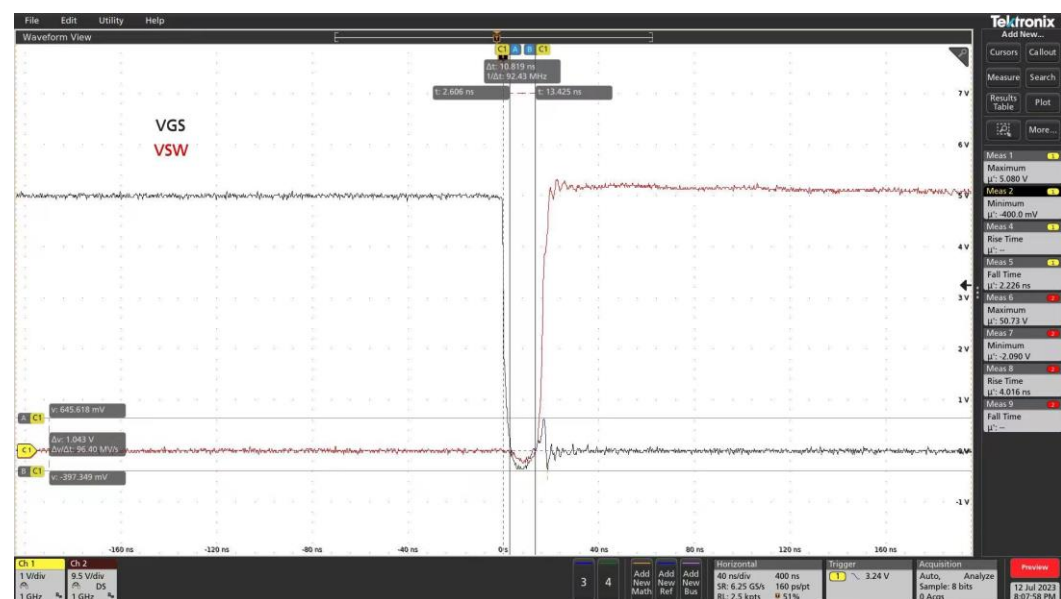**Rg_on=2.2Ω，Rg_off=0Ω**

Result

SW Edge：

Falling time=3.718ns

Falling Overshoot=-4.75V

LG Edge：

Rising time=21.15ns，

Test conditions

Buck Mode

Vin=48Vdc

Vout=12Vdc

Iout=23A

fsw=600kHz

Airflow=1400LFM

Rg_on=2.2Ω，Rg_off=0Ω

Result

SW Edge：

Rising Overshoot=2.73V

Rising time=4.016ns

LG Edge：

Falling time=2.226ns

Appendix
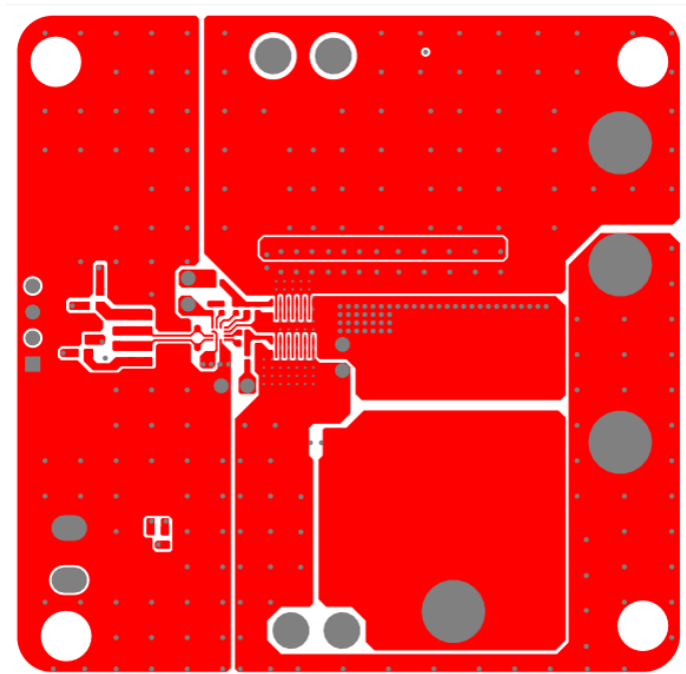
Appendix A. PCB Layout
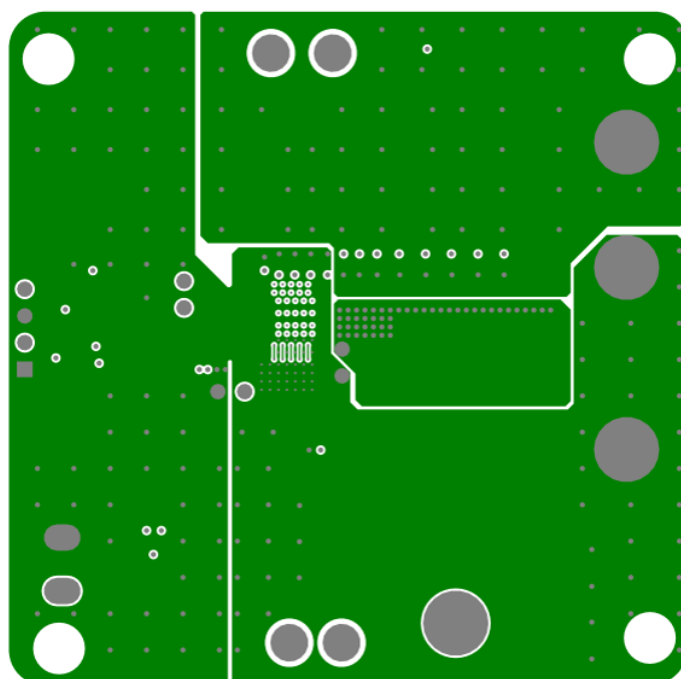

Figure 10 The top layer of INNEHB100C1

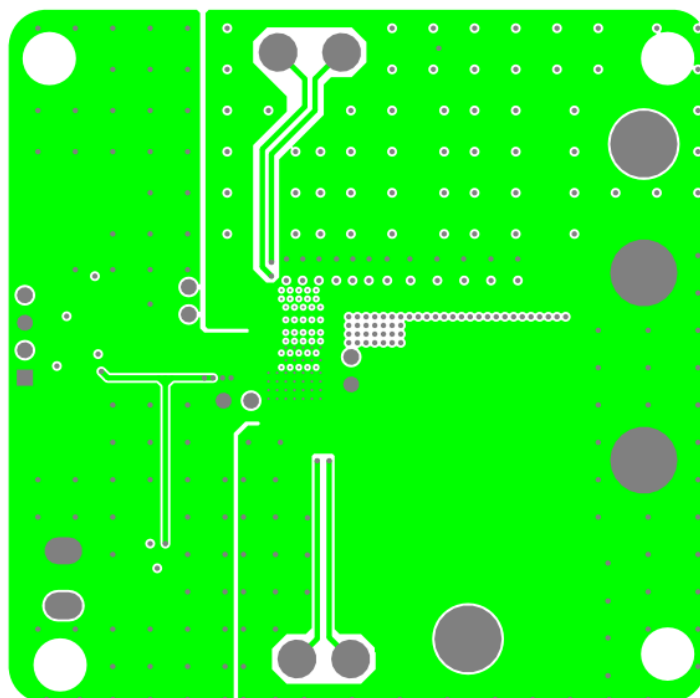Figure 11 The first middle layer of INNEHB100C1

Figure 12 The second middle layer of INNEHB100C1
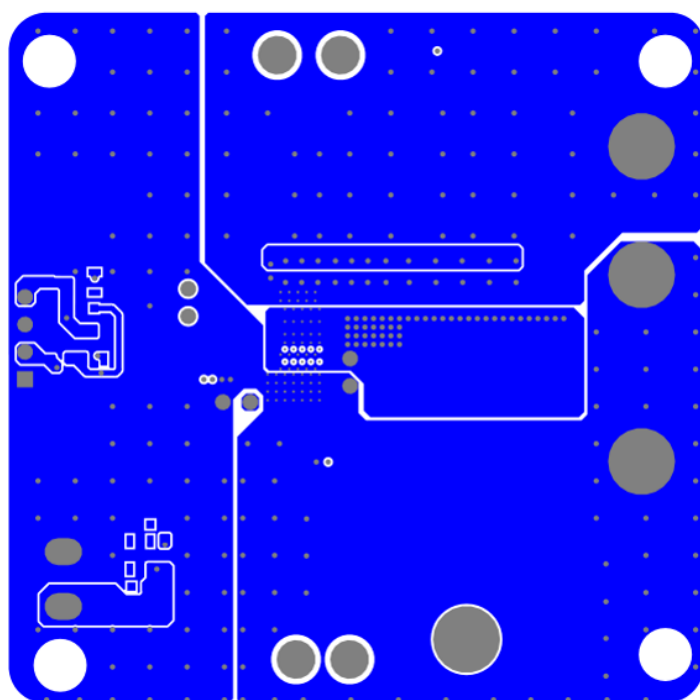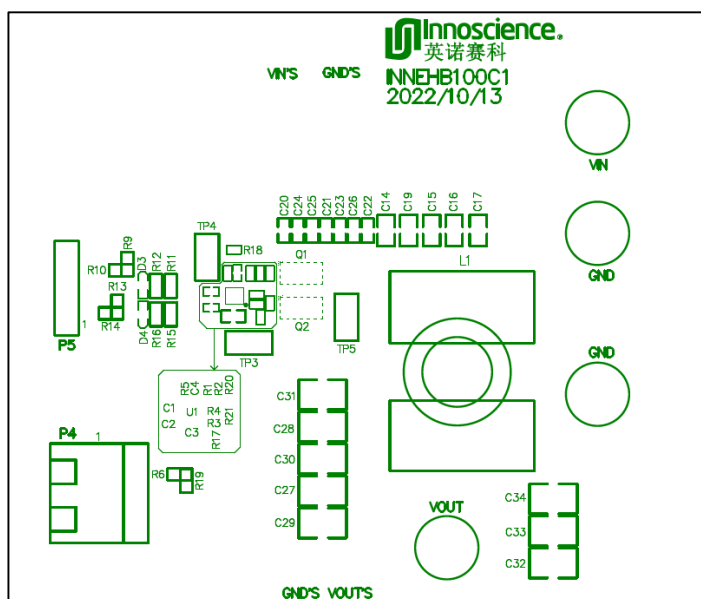

Figure 13 The bottom layer of INNEHB100C1

Figure 14 The top overlay of INNEHB100C1

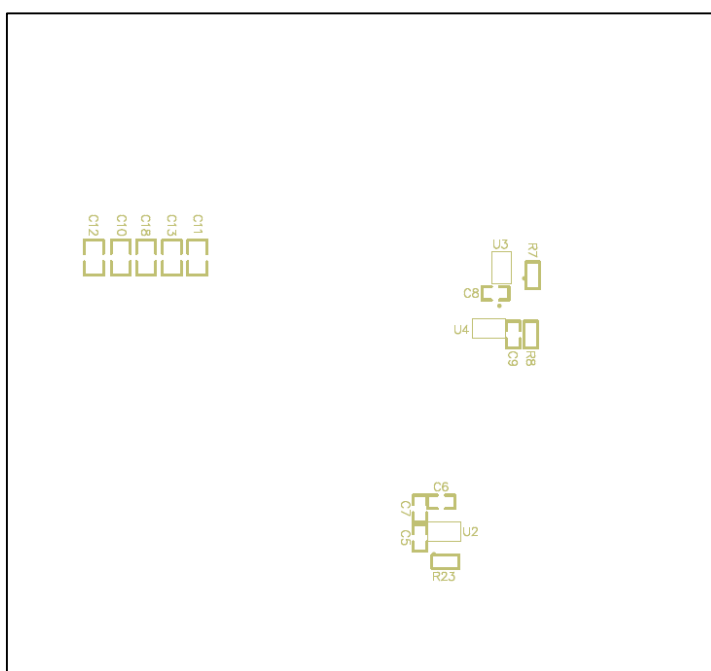Figure 14 The bottom overlay of INNEHB100C1

Appendix B. BOM

Table 2 BOM

Designator	Part Number	Manufacturer	Description	Footprint	Quantity
C1, C2	0402N201J500CT	WALSIN	CAP, 200pF/50V, ±5%, C0G	C0402	2
C3	TMK107BBJ475KA-T	TAIYO YUDEN	CAP, 4.7uF/25V, ±10%, X5R	C0603	1
C4	CGA2B3X7R1E104KT0Y0F	TDK	CAP, 100nF/25V, ±10%, X7R	C0402	1
C5, C6	CC0603KRX5R8BB225	YAGEO	CAP, 2.2uF/25V, ±10%, X5R	C0603	2
C7	TMK107BJ105KA-T	TAIYO YUDEN	CAP, 1uF/25V, ±10%, X5R	C0603	1
C8, C9	CC0603KRX7R8BB104	YAGEO	CAP,100nF/25V, ±10%, X7R	C0603	2
C10, C11, C12, C13, C14, C15, C16, C17, C18, C19	GCM21BC72A105KE36L	MURATA	CAP,1uF/100V, ±10%, X7S	C0805	10
C20, C21, C22, C23, C24, C25, C26	CL10B104KC8NNNC	SAMSUNG	CAP,100nF/100V, ±10%, X7R	C0603	7
C27, C28,C30,C31,C34	GRM32EC72A106KE05K	MURATA	CAP,10uF/100V, ±10%, X7S	C1210	5
C29,C32,C33	EMPTY		CAP	C1210	3
R1, R4	RC0402FR-072R2L	YAGEO	Res, 2.2Ω, ±1%	R0402	2
R2, R3, R5, R17, R18	RC0402JR-070RL	YAGEO	Res, 0Ω, ±1%	R0402	5
R6, R9, R13	ERJ3GEY0R00V	PANASONIC	Res, 0Ω, 100mW	R0603	3
R7, R8	ERA3AEB103V	PANASONIC	Res, 10KΩ, ±0.1%	R0603	2
R10, R11, R14, R15, R19	EMPTY		Res	R0603	5
R12	RC0603FR-07200RL	YAGEO	Res, 200Ω, ±1%	R0603	1
R16	RC0603FR-07360RL	YAGEO	Res, 360Ω, ±1%	R0603	1
R20, R21	ERA2AED103X	PANASONIC	Res, 10KΩ, ±0.5%	R0402	2
L1	EMPTY		Inductance		1
D3, D4	SDM03U40-7	DIODES	Schottky, 30V, 30mA	SOD-523	2
Q1, Q2	INN100W027A	INNOSCIENCE	GAN FETs, 100V/2.7mΩ	WLCSP 4.45mm×2.30mm	2
U1	uP1966E	UPI SEMICONDUCTOR	Dual-Channel Gate Driver	WLCSP1.6x1.6-12B	1
U2	TPS70950DBVR-TP	TECH PUBLIC	LDO voltage regulators , fixed 5V output,	SOT-23	1
U3	SN74LVC1G08DBVR	TEXAS INSTRUMENTS	Single 2-Input Positive-AND Gate	SOT-23	1
U4	NC7SZ00M5X	ONSEMI	Two-Input NAND Gate	SC-74A	1

Revision History

Date	Author	Versions	Description	Check
9/8/2023	YubinHuang	1.0	First edition	AE Team

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⚠ Disclaimer:

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